BITS-Pilani Dubai, Dubai International Academic City, Dubai
III Yr. B.E.(Hons.) First Semester Academic Year 2010 – 2011

COMPREHENSIVE EXAMINATION (Closed Book) - MICROELECTRONIC CIRCUITS

Course No.	: EEE C424 / ECE C313 / INSTR C313	Date	: 26.12.2010
Duration	: 3 Hrs	Max Marks	: 120
		Weightage	: 40%

NOTE: 1. Answer Part A and Part B of each question in **Two separate answer books**.
2. Make assumptions, if any, but explicitly indicate the assumptions made.

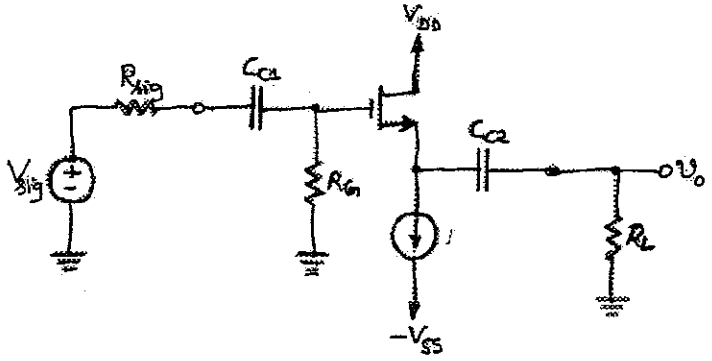
* * * * *

PART A

1) With a neat circuit diagram of a single stage CG amplifier and using its small signal analysis derive an expression for (a) an overall voltage gain, (b) input resistance and (c) output resistance (10 M)

2) For the circuit shown below, find R_{in}, A_{vo}, A_v, G_V and R_{out}, both (a) with r_0 and (b) without r_0. if g_m=1mA/V, r_0=100KΩ, R_{sig}=2MΩ, R_L=30KΩ. and RG=4.7MΩ

(6 + 4 = 10M)



3) Starting from fundamentals derive an expression for f_T of a typical MOSFET. Also calculate the same if the device's V_{OV}=0.25V, C_{gs}=20fF, C_{gd}=5fF and is operating at I_D=100μA. (6+2=8M

4) Draw the (a) circuit diagram of a BJT differential amplifier and (b) its transfer characteristics. Also explain why the shape for the transfer characteristics. (6M)

5) Design a Butterworth low-pass filter to have: f_p=10KHz, A_{max}=2dB, f_s=15kHz, and A_{min}=15dB. Estimate the attenuation it provides at 20kHz. (3+3+4+2=12)

6) Neglecting the effects of finite V_{BE} and V_{CEsat} find: (2+2+2=6M)
   a) maximum sine wave output power available
   b) average power drawn from each of the power supplies and
   c) power conversion efficiency

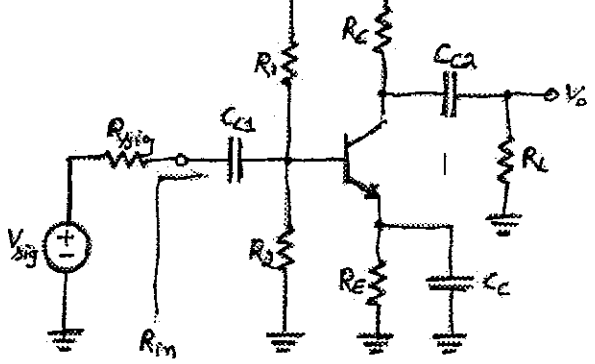
   of a Complementary BJT class B output stage having ±10V power supply and a 100Ω load resistance.

7) It is required to ensure safe operation at 30W of a power transistor which at T_{Jmax}=180°C can dissipate 50W at a case temperature of 50°C. Find the (3+3+2=8M)
   a) necessary heat sink temperature, if the device is connected to a heat sink using an insulating washer whose thermal resistance of 0.6°C/W.
   b) required thermal resistance of the heat sink, if ambient temperature is 40°C .
   c) length of the required extruded-aluminum-finned heat sink, whose thermal resistance in still air is 4.5°C/W per centimeter of its length?

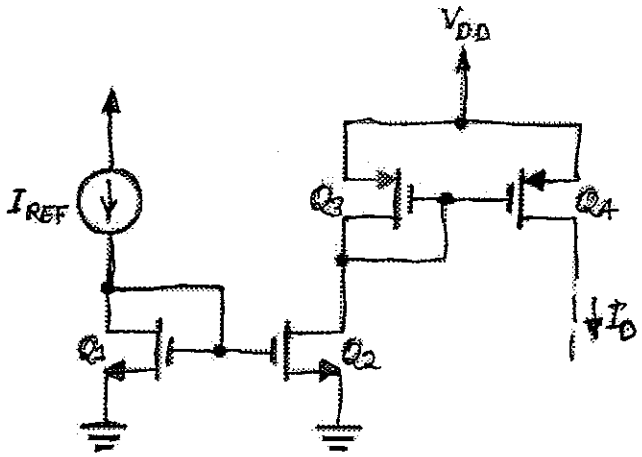
PART B

1) A BJT whose β = 220 is biased to operate in the active mode at a dc collector current of 2.0 mA. Draw each of following model and compute its parameters: (2.5x4=10M)
   a) Simplified hybrid-π VCCS model
   b) Simplified hybrid-π CCCS model
   c) VCCS representation of T-model
   d) CCCS representation of T-model

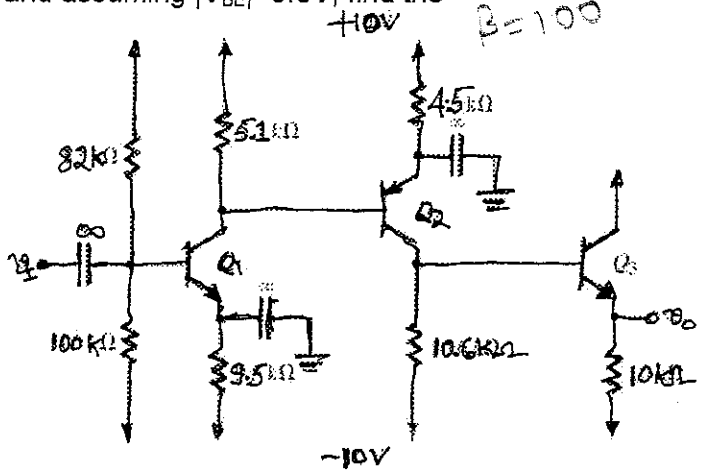
2) For the amplifier in the figure below whose component values are: R_{sig}=5KΩ, R_1=39KΩ, R_2=27KΩ, R_E=3.3KΩ, R_C=4.7KΩ, R_L=5.6KΩ, V_{CC}=10V, let C_{C1}=C_{C2}=2μF, and C_E=25μF. Assume that device's β_{dc}=100 and r_O=300KΩ. Find amplifier's break frequencies: (a)f_{P1}, (b)f_{P2} and (c)f_{P3} (resulting from C_{C1}, C_{C2} and C_E respectively) and (d) its lower 3-dB frequency f_L. (4x2=8M)



3) For the current steering circuit shown in figure below, find I_O in terms of I_{REF} and device (W/L) ratios. (10M)



4) Figure below shows a three stage amplifier in which the stages are directly coupled. Neglecting early effect and assuming $|V_{BE}|$=0.6V, find the (5x2=10M)



a) dc bias current in each of the three transistors and
b) dc voltage at the output.
c) input resistance
d) output resistance
e) voltage gain v_o/v_i

5) a) An amplifier with open-loop voltage gain A_V=1500 ± 150 is available. It is necessary to have an amplifier whose voltage gain more than ±0.2%. Find the reverse transmission factor β of the feedback network used and also the gain with feedback. (4M)
b) A series-shunt feedback amplifier employs a basic amplifier with input and output resistances of 1.5KΩ each and gain of A = 1500 V/V. The feedback factor is 0.2 V/V. Find A_f, R_{if} and R_{of} of the closed-loop amplifier. (1+1.5+1.5=4M)

6) An amplifier has a dc gain of 10^5 and poles at 10^5 Hz, and 3.16×10^5Hz and 10^6 Hz. Find the value of β and the corresponding closed loop gain for which a phase margin of 45° is obtained. (6M)

7) Illustrate the structure and special features of the following compound devices (a)Darlington pair (b)Totem-pole Configuration and (c) Cascode amplifier (3+2+3=8M)

******) ALL THE BEST(******

BITS-Pilani Dubai, International Academic City, Dubai

I – Semester Academic Year 2010-11

Evaluation Component : **TEST – II (Open Book)**

EEE C424 / ECE C313 / INSTR C313 MICROELECTRONIC CIRCUITS

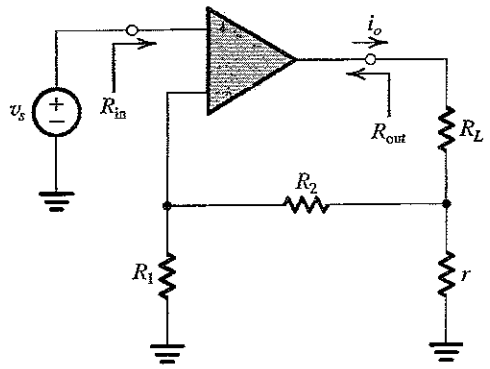
Date : 21st November 2010 **Maximum Marks: 60**

Duration: 50 mts. **Weightage :20%**

Note:- 1. ANSWER ALL the Questions with **"most appropriate answer(s)"**
2. Wherever required, make reasonable assumptions and **indicate explicitly the assumptions made**, if any.
3. Use Semi-log Graph sheet, wherever required.

- - -

1. Identify the (a)Feedback topology and (b)the circuit elements that constitute feedback network in the feedback amplifier circuit shown the figure below. Compute (c) Transfer gain(A_f) of the feedback amplifier; and the values of (d)R_{in} & (e)R_{out} – as shown in the figure assuming OPAMP's internal parameters as: open loop voltage gain (μ)=10^5 V/V; differential input resistance (R_{id}) =10KΩ; output resistance r_o=100Ω and given that: R_L=1KΩ, r=100Ω, R_2=1KΩ and R_1=100Ω. If R_1 is made infinite and OPAMP's μ drifts to it's a new value = 10^4 V/V, also find (f)A_f, (g)R_{in} and (h)R_{out}. (0.5+0.5+3x3+2x3=16M)



2. An NMOS differential amplifier is operated at a bias current of I of 0.5 mA and has W/L ratio of 50, $\mu_n C_{ox}$= 250 μA/V^2, V_A = 10V and R_D is 4KΩ find V_{ov}, g_m, r_o and A_d. (5M)

3. A dc amplifier has two poles and an open loop gain of 1000. One of the poles is at 1 KHz (the dominant one) while the other is at a location controllable by the designer. Find the β and the required value of pole if this amplifier is required to be connected in a negative feedback loop to provide a dc closed loop gain of 100 and a maximally flat response. (5+5=10M)

4. Sketch the polar plot of the loop gain βA, indicating in each case whether or not the closed loop amplifier is stable, for a three-pole feedback amplifier with a dc gain (without feedback) A_o = -1000, and open-loop poles at f_1=0.5 MHz, f_2=1MHz, and f_3=2 MHz assuming (a) β = - 0.005; (b) β = - 0.02; (c) Also find the maximum value of β for which the amplifier is stable? (3+3+3=9M)

5. A three-pole feedback amplifier has a dc gain without feedback of -10^4. All the three open-loop poles are at f=2 MHz. (a) what is the maximum value of β for which the amplifier is stable? (b) If one of the poles is shifted to f_1=100 KHz, using the value of β found in (a) compute the gain margin of the modified circuit. (5+5=10M)

6. For NMOS differential pair with common mode voltage v_{CM} applied as shown in the assuming V_{DD}=V_{SS}=2.5V k_n'W/L=3mA/V^2. V_t=0.7V, I=0.2mA, R_D=5KΩ and neglect the channel length modulation. Find (a) Find V_{OV} and V_{GS} for each transistor (b) v_s, i_{D1}, v_{D1} and v_{D2} if V_{CM}=0 (c) Repeat (b) for v_{CM}=+1V, (d) Repeat (b) v_{CM}=-1V, (e)What is the highest value of v_{CM} for which Q_1 and Q_2 will remain in saturation? (5x2=10M)

**** ALL THE BEST ****

BITS-Pilani Dubai, Dubai International Academic City, Dubai

III Yr. B.E.(Hons.) FIRST SEMESTER 2010 – 2011

TEST-I (Closed Book)

MICROELECTRONIC CIRCUITS

Course Code : **EEE C424 / ECE C313 / INSTR C313** Date: **10.10.10**
Course Title : **Microelectronic Circuits** Max Marks: **60**
Duration : **50 minutes** Weightage: **20%**

NOTE: 1. Answer ALL questions.
2. Make assumptions, if any, but explicitly indicate the assumptions made.

* * * * *

1) Define any SIX of the following terms with reference to electronic amplifier circuits:
   (i) Voltage Gain
   (ii) Bandwidth
   (iii) Amplifier saturation
   (iv) Maximum signal handling capacity
   (v) Efficiency
   (vi) AC Load Line
   (vii) Amplifier Loading
   (viii) Lower 3dB Frequency
   (ix) Figure of merit (6.0 M)

2) List the all the steps to perform low frequency small signal analysis of an amplifier circuit employing BJT or FET, indicating the typical assumptions made during the analysis. (4.0 M)

3) List any six important considerations in choosing the BIAS POINT while designing of a BJT Amplifier (6.0 M)

4) Draw the circuit of BJT Self Bias and Fixed Bias schemes. Justify why are the biasing schemes named so. (3+3=6M)

5) Derive an expression for magnitude response of Single Time Constant which do not attenuate low frequency components of the signal fed to its input and deduce an expression for its 3-dB cut-off frequency. (3+3=6.0 M)

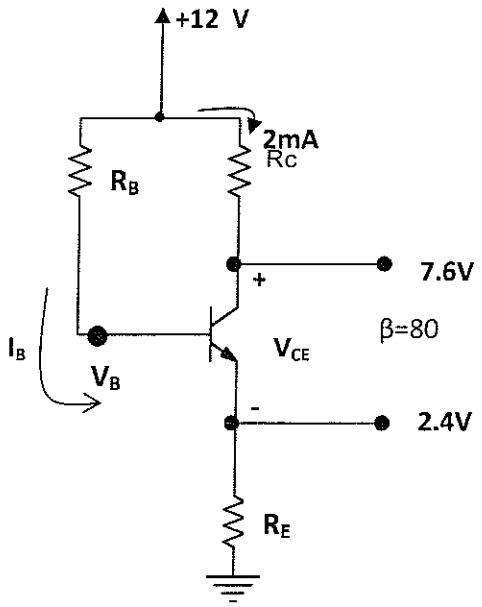
6) Derive expressions for A_v, A_{vo}, A_{is} and G_v of a Common Emitter amplifier and indicate all characteristic changes due to inclusion of a small value of un-bypassed emitter resistance (6+3=9M)

7) A BJT Common Emitter Amplifier with R_C=10 kΩ is connected between a source with R_s=5 kΩ, and a load of R_L=5 kΩ. Assuming that the parameters of the BJT model are: r_n=2.5 kΩ, g_m=40mA/V, r_0=100 kΩ,
   a) Derive an expression for overall voltage gain (3M)
   b) Find the magnitude of overall voltage gain. (3M)
   c) Recalculate the magnitude of overall voltage gain neglecting r_o (3M)

(Please Turn Over)

8) Draw the h-parameter model of a BJT used in CE Configuration and define all the four parameters, and indicate how each of the four model parameters can be obtained from BJT characteristics. (1+1+4=6 M)

9) Given the following Circuit shown in Fig. 1. below, find R_C, R_E, R_B, V_{CE}, V_B (1.5x4+2=8M)



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ALL THE BEST

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A

BITS-Pilani Dubai, Dubai International Academic City, Dubai
III Yr. B.E.(Hons.) FIRST SEMESTER 2010 – 2011

QUIZ -2

MICROELECTRONIC CIRCUITS

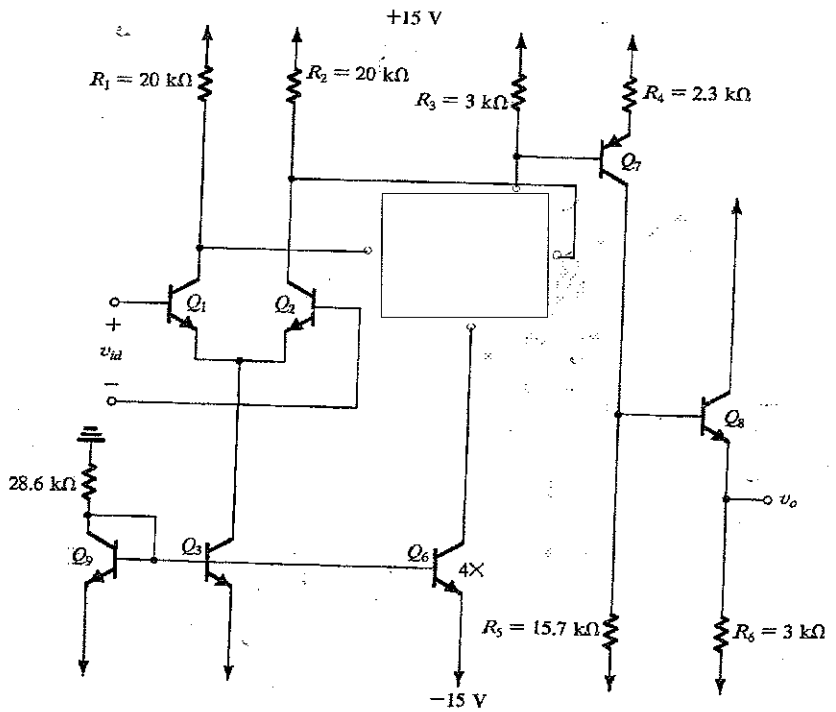
Course Code: **EEE C424 / ECE C313 / INSTR C313** Date: **14.12.10**
Course Title : **Microelectronic Circuits** Max Marks: **30**
Duration : **50 minutes** Weightage: **10%**

NOTE: 1. Answer ALL questions.
2. Make assumptions, if any, but explicitly indicate the assumptions

Q1) Identify the incorrect statements with respect to multistage amplifier (2M)

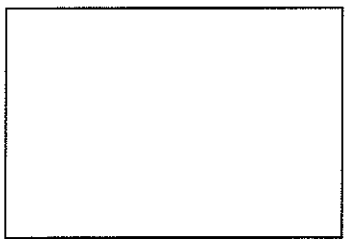
a. Output stage is always a differential amplifier.
b. DC level shifting is done in the intermediate stage
c. Input stage is responsible for the bulk gain
d. Output stage is a power amplifier

Q2) Complete the following circuit diagram by drawing the missing circuit elements in square mark (2M)



Q3)What is the overall 3dB frequency of six non interacting cascading stages of high pass filters, each having 3dB high frequency of 5KHz (2M)
Ans: _____

Q4) Draw a Darlington pair using BJT (1M)



Q5) Find the input voltage required to a three stage cascaded voltage amplifier, with each stage having 20dB of gain, to get an output voltage of 2.5V (2M)

Ans: _____

Q6) Define Total Harmonic Distortion (THD) in one sentence. (1M)

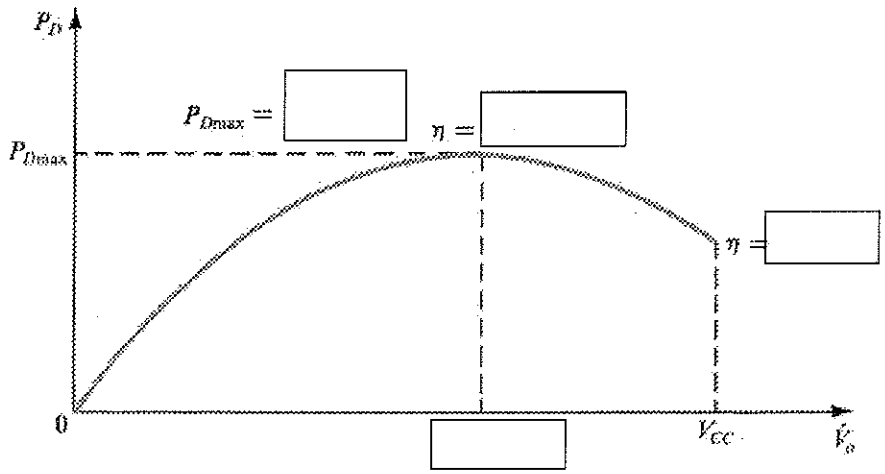
Q7) Draw the collector current waveform for the Class B Amplifier (1M)

Q8) The expression for the power conversion efficiency of class A amplifier is _____. And under _____conditions maximum efficiency of _____ is obtained. (3M)

Q9) For the class B output stage amplifier V_{cc}=10V, and RL=20Ω. If the output is sinusoid with 6.5 V peak amplitude, Find (1x4=4M)

a. The output power = _____
b. Average power drawn from each supply= _____
c. The power efficiency obtained at this output stage= _____
d. The peak current supplied by V_I, assuming β_N=100= _____

Q10) Fill the required answers in the square boxes shown in the following figure , which shows the power dissipation of a class B output stage versus amplitude of the output sinusoid. (1X4=4)



Q11) A BJT is specified to have T_{JMAX}=100°C, and to be capable of dissipating maximum power of 40W at T_C=25°C and 2W at T_A=25°C. Above 25°C, the maximum power dissipation is to be derated linearly with θ_{JC}=2.12°C, and θ_{JA}=60.5°C. Find

a. The maximum power that can be dissipated safely by this transistor, when operated in the free air at 45°C.

Ans: _____

b. The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C, but with a heat sink for which θ_{CS}=0.4°C/W and θ_{SA}=3°C/W.

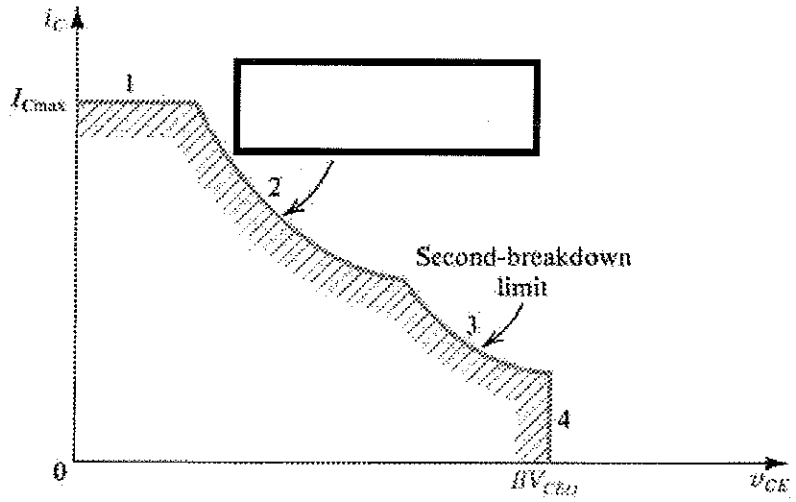
Ans: _____

(1+2=3M)

Q12) Draw the circuit diagram for the biasing class AB amplifier using diodes. (2M)

Q13) In class B amplifier , there exist a range of input voltage v_I centered around zero where both the transistor are cut off and v_0 is _____. This _____ results in the cross over distortion. (2M)

Q14) Following is a safe operating area of BJT, fill the proper answer for the region 2 in the square box shown. (1M)



B

BITS-Pilani Dubai, Dubai International Academic City, Dubai
III Yr. B.E.(Hons.) FIRST SEMESTER 2010 – 2011

QUIZ -2

MICROELECTRONIC CIRCUITS

Course Code: **EEE C424 / ECE C313 / INSTR C313** Date: **14.12.10**
Course Title : **Microelectronic Circuits** Max Marks: **30**
Duration : **50 minutes** Weightage: **10%**

NOTE: 1. Answer ALL questions.
2. Make assumptions, if any, but explicitly indicate the assumptions

Q1) For the class B output stage amplifier V_{cc}=12V, and R_L=25Ω. If the output is sinusoid with 6.5 V peak amplitude, Find (1x4=4M)

a. The output power = _____
b. Average power drawn from each supply= _____
c. The power efficiency obtained at this output stage= _____
d. The peak current supplied by V_I, assuming β_N=100= _____

Q2)What is the overall 3dB frequency of four non interacting cascading stages of high pass filters, each having 3dB high frequency of 5KHz (2M)

Ans: _____

Q3) Draw a Darlington pair using FET (1M)

Q4) Find the input voltage required to a three stage cascaded voltage amplifier, with each stage having 30dB of gain, to get an output voltage of 4.5V (2M)

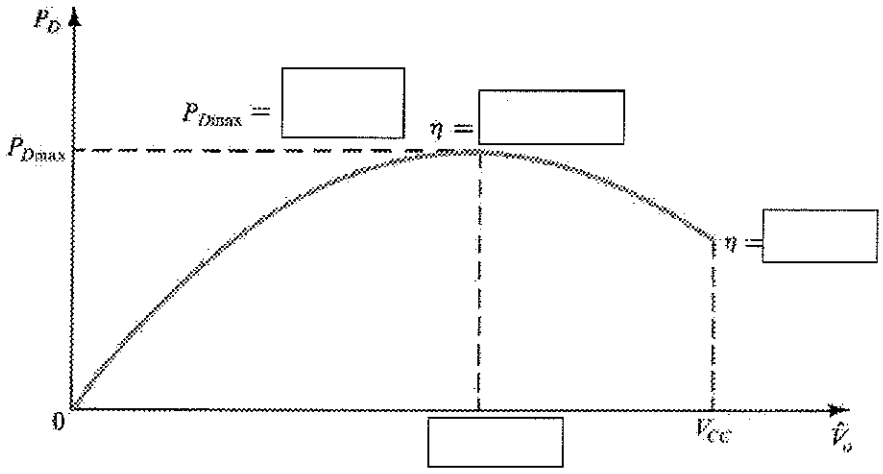
Ans: _____

Q5) Define Total Harmonic Distortion (THD) in one sentence. (1M)

Q6) Draw the collector current waveform for the Class C Amplifier (1M)

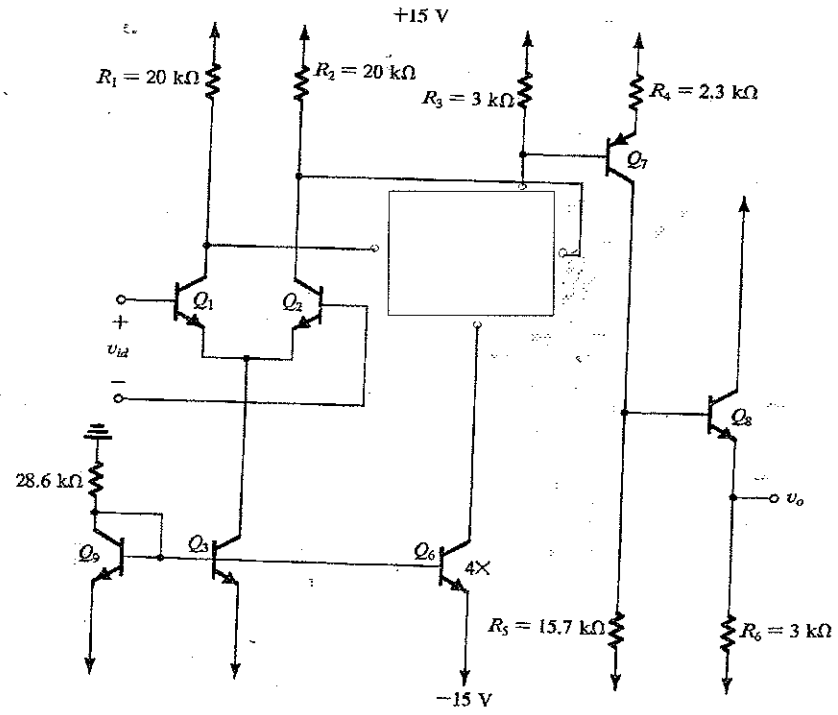
Q7) Expression for the power conversion efficiency of class A amplifier is _____, and under _____conditions maximum efficiency of _____ is obtained. (3M)

Q8) Fill required answers in the square boxes shown in the following figure, which shows the power dissipation of a class B output stage versus amplitude of the output sinusoid. (1X4=4)



Q9) In class B amplifier , there exist a range of input voltage v_I centered around zero where both the transistor are cut off and v_O is _____ This dead band results in the _____. (2M)

Q10) Complete the following circuit diagram by drawing the missing circuit elements in square mark (2M)



Q11) A BJT is specified to have T_{JMAX}=100°C, and to be capable of dissipating maximum power of 40W at T_C=25°C and 2W at T_A=25°C. Above 25°C, the maximum power dissipation is to be derated linearly with θ_{JC}=2.12°C, and θ_{JA}=60.5°C. Find

a. The maximum power that can be dissipated safely by this transistor, when operated in the free air at 45°C.

Ans: _____

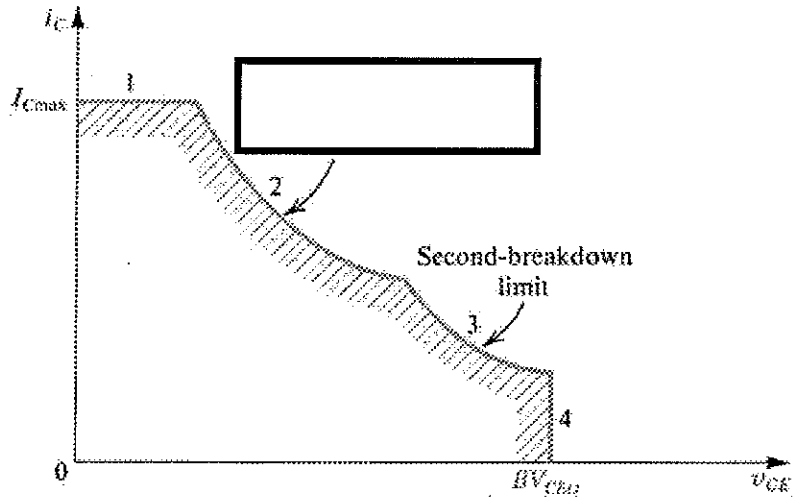
b. The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C, but with a heat sink for which θ_{CS}=0.4°C/W and θ_{SA}=3°C/W.

Ans: _____

(1+2=3M)

Q12) Draw the circuit diagram for the biasing class AB amplifier using diodes. (2M)

Q13) Following is safe operating area plotted on i_C-v_{CE} characteristics of a BJT, fill the proper answer for the region 2 in the square box shown. (1M)



Q14) Identify the incorrect statements with respect to multistage amplifier

(2M)

a. DC level shifting is done in the intermediate stage
b. Input stage is responsible for the bulk gain
c. Output stage is a power amplifier
d. Output stage is always a differential amplifier.

Student Name: _____ BITS ID No.: _____

BITS-Pilani Dubai, International Academic City, Dubai

I – Semester Academic Year 2010-11

A

Evaluation Component : **QUIZ - I**

EEE C424 / ECE C313 / INSTR C313 MICROELECTRONIC CIRCUITS

Date : 3rd November 2010 **Maximum Marks: 30**

Duration: 25 mts. **Weightage :10%**

Note:- 1.Respond ALL questions
2. Provide **"most appropriate answer(s)"** for each question.
3. Indicate explicitly the assumptions if any.
4. All questions carry 1 mark unless otherwise indicated

- - -

1. Express the feedback amplifier's transfer gain, A_f = _____ (1M)
2. Match the following feedback topology shown under I with the corresponding term under II ...by indicating the serial no. of I in the braces: "[ ]" of II. (2M)

I	II	
A. Series Series	current mixing and current sampling	[ ]
B. Shunt Series	current mixing and voltage sampling	[ ]
C. Shunt Shunt	voltage mixing and current sampling	[ ]
D. Series Shunt	voltage mixing and voltage sampling	[ ]

3. In a MOSFET , the thickness of the oxide layer is 10nm, and permittivity of the silicon dioxide is 3.45×10^{-11} F/m, what is the capacitance per unit area C_{ox}. (2 M)

4. In an FET, expression for i_D in the saturation region is: _____ in which, i_D is:_____I K_n' is : _____; W is: _____; L is:_____; v_{GS} is : _____ and V_t is: _____ (1+0.5x6=4M)
5. Given below are the distinguishing features of an FET over BJT for its use as an amplifier. Indicate "True" or "False" in the parenthesis given against each. (3M)
   A. FET occupies lesser space during IC fabrication [ ]
   B. FET is less immune to noise than BJT [ ]
   C. FET consumes more power than BJT [ ]
   D. FET offers a high input resistance over BJT [ ]
   E. FET offers higher voltage gain than BJT [ ]
   F. FET do not offer response without a stimulus unlike BJT [ ]
6. The Voltage gain of a CS amplifier employing a device whose g_m = 10 mA/V; r_0 = 150 KΩ with an R_L=15 KΩ and R_D=1 KΩ is _____. (1 M)
7. Draw the high frequency Hybrid-π model of a MOSFET in which body effect is negligible (the source is connected to the substrate) (3 M)

8. An amplifier with open-loop gain Av=1,000±100 is available. It is necessary to have an amplifier whose voltage gain varies by no more than ±0.1 percent. Find β and A_{vf}. (2 M)

(Please Turn Over)

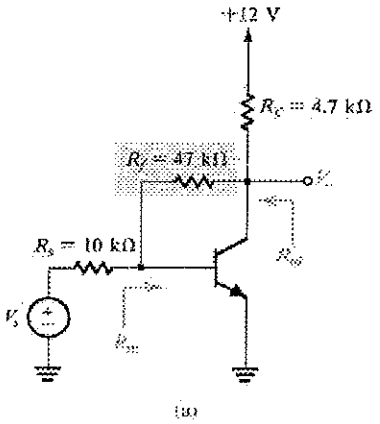
9. In determining the loop gain Aβ through an approach in which conceptual feed back loop is broken and a test signal (as appropriate) is applied, express Aβ in terms of Open & Short circuit transfer functions (T_{oc} & T_{sc} respectively) and also provide expressions to find T_{oc} and T_{sc}. (0.5x 7=3.5 M)

Aβ = ; T_{sc} = ; T_{oc} = where in

____ is _____ ; ____ is _____ ;

____ is _____ ; ____ is _____

10. If the two poles of a feedback amplifier are on the imaginary axis and are complex in nature then they occur as a _____ pair and the amplifier is said to have _____ response. (0.5+0.5=1M)
11. Identify the feedback topology of the circuit given below. Draw the A Circuit in the space provided below. If g_m is 60 mA/V; BJT's β_{dc} =100; Compute A and β for this feedback amplifier. (1+0.5+0.5=2 M)



(a)

A Circuit is:

A = _____; β = _____

12. The Gain Margin is defined as the value of_____in dB at which the phase angle of _____ is _____degrees. (1.5 M)
13. The Phase margin is _____ degrees minus _____ at the frequency at which _____ is unity. (1.5 M)
14. In determining the stability of a feedback amplifier, if the Nyquist plot of _____ encircles _____, the amplifier will be unstable. (1 M)
15. Draw the root locus diagram of a feedback amplifier having two poles on the negative real axis and comment on the stability of the amplifier. (1+0.5=1.5 M)

Root-Locus-Diagram

A comment on the Stability of the amplifier:

_____

_____

_____

**** ALL THE BEST ****

Student Name: _____ BITS ID No.: _____

BITS-Pilani Dubai, International Academic City, Dubai

I – Semester Academic Year 2010-11

B

Evaluation Component : **QUIZ - I**

EEE C424 / ECE C313 / INSTR C313 MICROELECTRONIC CIRCUITS

Date : 3rd November 2010 **Maximum Marks: 30**

Duration: 25 mts. **Weightage :10%**

Note:- 1.Respond ALL questions
2. Provide **"most appropriate answer(s)"** for each question.
3. Indicate explicitly the assumptions if any.
4. All questions carry 1 mark unless otherwise indicated

- - -

1. Match the following feedback topology shown under I with the corresponding term under II ...by indicating the serial no. of I in the braces: "[ ]" of II. (2M)

I	II	
A. Shunt Series	current mixing and voltage sampling	[ ]
B. Series Series	current mixing and current sampling	[ ]
C. Series Shunt	voltage mixing and voltage sampling	[ ]
D. Shunt Shunt	voltage mixing and current sampling	[ ]

2. In an FET, expression for i_D in the saturation region is: _____ in which, i_D is:_____| K_n' is : _____; W is: _____; L is:_____; v_{GS} is : _____ and V_t is: _____ (1+0.5x6=4M)

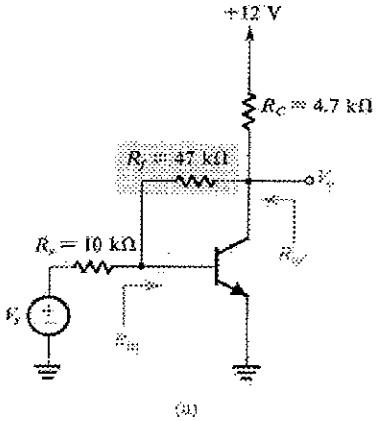
3. Given below are the distinguishing features of an FET over BJT for its use as an amplifier. Indicate "True" or "False" in the parenthesis given against each. (3M)
   a. FET do not offer response without a stimulus unlike BJT [ ]
   b. FET occupies lesser space during IC fabrication [ ]
   c. FET offers a high input resistance over BJT [ ]
   d. FET is less immune to noise than BJT [ ]
   e. FET consumes more power than BJT [ ]
   f. FET offers higher voltage gain than BJT [ ]

4. In a MOSFET , the thickness of the oxide layer is 10nm, and permittivity of the silicon dioxide is 3.45×10^{-11} F/m, what is the capacitance per unit area C_{ox}. (2 M)

5. Express the feedback amplifier's transfer gain, A_f = _____ (1M)

6. The Phase margin is _____ degrees minus _____ at the frequency at which _____ is unity. (1.5 M)

7. Identify the feedback topology of the circuit given below. Draw the A Circuit in the space provided below. If g_m is 60 mA/V; BJT's β_{dc} =100; Compute A and β for this feedback amplifier. (1+0.5+0.5=2 M)



(a)

A Circuit is:

A = _____; β = _____

(Please Turn Over)

8. Draw the high frequency Hybrid-π model of a MOSFET in which body effect is negligible (the source is connected to the substrate) (3 M)

9. An amplifier with open-loop gain Av=1,000±100 is available. It is necessary to have an amplifier whose voltage gain varies by no more than ±0.1 percent. Find β and A_{vf}. (2 M)

10. In determining the loop gain Aβ through an approach in which conceptual feed back loop is broken and a test signal (as appropriate) is applied, express Aβ in terms of Open & Short circuit transfer functions (T_{oc} & T_{sc} respectively) and also provide expressions to find T_{oc} and T_{sc}. (0.5x 7=3.5 M)

Aβ = ; T_{sc} = ; T_{oc} = where in

____ is _____ ; ____ is _____ ;

____ is _____ ; ____ is _____

11. Draw the root locus diagram of a feedback amplifier having two poles on the negative real axis and comment on the stability of the amplifier. (1+0.5=1.5 M)

Root Locus Diagram	A comment on the Stability of the amplifier:
	_____
	_____
	_____

12. The Gain Margin is defined as the value of_____in dB at which the phase angle of _____ is _____degrees. (1.5 M)
13. If the two poles of a feedback amplifier are on the imaginary axis and are complex in nature then they occur as a _____ pair and the amplifier is said to have _____ response. (0.5+0.5=1M)
14. The Voltage gain of a CS amplifier employing a device whose g_m = 10 mA/V; r_o = 150 KΩ with an R_L=15 KΩ and R_D=1 KΩ is _____. (1 M)
15. In determining the stability of a feedback amplifier, if the Nyquist plot of _____ encircles _____, the amplifier will be unstable. (1 M)

**** ALL THE BEST ****