BITS, PILANI – DUBAI

International Academic City, Dubai

Year III – Semester I 2010-2011

COMPREHENSIVE EXAMINATION

Course No.: CS C391 / INSTR C 391 **Course Title: DECO**

Date: December 27, 2010 Time: 3 Hours Max. Marks = 80

Clearly indicate the assumptions made if any. All logic used are positive logic

Answer Part A and Part B separately

Calculators are not allowed

PART A

1 a) Draw the logic diagram of a four bit gray to binary code converter. Write the equivalent binary code for the gray code **1101011**

b) Perform the BCD addition for the decimal numbers (678 + 429) and verify the result

c) What are the maximum and minimum decimal numbers that can be represented using 8 bits in two's complement form (2 + 3 + 2)

2 a) Design a 4 input priority encoder with input D_0 having the highest priority and input D_3 having the lowest priority. 5M

b) A combinational circuit inputs two 2-bit unsigned numbers and outputs a 3-bit unsigned number that represents the sum of the two numbers.
i) Draw the truth table for the problem
ii) Get the output expressions using K-map.
iii) Draw the combinational circuit for the expressions obtained. (2 + 3 +3)

3 a) Use a 4 x 1 multiplexer to implement the following function, assuming that all inputs and outputs are active high. It is required that minimum external logic gates to the MUX be used in each case and that the data select inputs be A and B. Assume A is the MSB. $F(A,B,C,D) = \Sigma(0,4,5,7,8,9,13,15)$ 5M

b) Use a 4 x 16 line active low decoder and two input external NAND gates to implement the above function given in Q3 a). 5M

4 a) Derive the PLA programming table for BCD to X-s 3 code converter. Optimize the no. of product terms for true outputs. 5M

b) Draw a neat circuit and explain the function of each component of a tristated TTL NAND gate circuit 5M

PART B

5 a) Draw and explain the **logic diagram** of a 3bit x 2 bit word multiplier circuit. Explain the working of the circuit using the decimal data 7 x 2 5M

b) Explain the working of the computer algorithm for integer division using **Non-restoration method**. Show the operations using the example 11 / 3 in steps 5M

6 a) Draw the logic diagram of a 4: 1 multiplexer and write its HDL gate level description module named **4x1mux**. Also write a stimulus for the module 6M

b) What is the need for data transfer in I/O devices ? Explain the following with reference to I/O devices.

i) Modes of data transfer

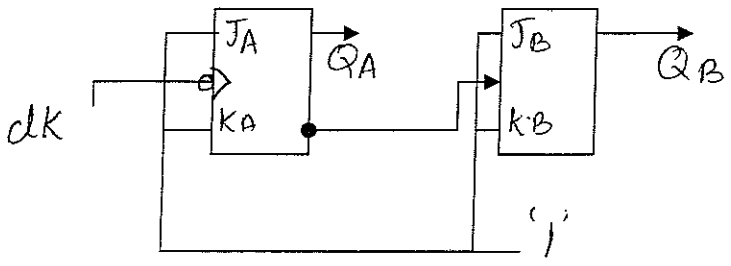
ii) Control of data transfer 2 + 2 M

7 a) Design a four bit universal shift register using D flip flops and multiplexers which will perform the following operations based on the function table given below.

No.	C_1 C_0	Function
1	0 0	Clear the register
2	0 1	Shift right
3	1 0	Shift left
4	1 1	Load new data

5M

b. For the asynchronous counter circuit shown in figure below, draw the complete timing diagram for eight clock pulses showing the clock inputs, Q_A and Q_B waveforms. Assume that Q_A and Q_B are initially cleared.



(1 + 2 + 2 M)

8 a) Design a synchronous BCD (mod – 10) counter using T flip flops. 4M

b. A synchronous sequential circuit has two T flip flops A and B. The flip flop input equations are given by

$T_A = A + B$ $T_B = A' + B$

i) Draw the logic diagram for the circuit.

ii) Tabulate the state table

iii) Derive the state equations for the flip flops A and B.

iv) What is the function of the circuit? 1.5 x 4 M

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Good Luck

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Dubai International Academic City

I semester III Year 2010-2011

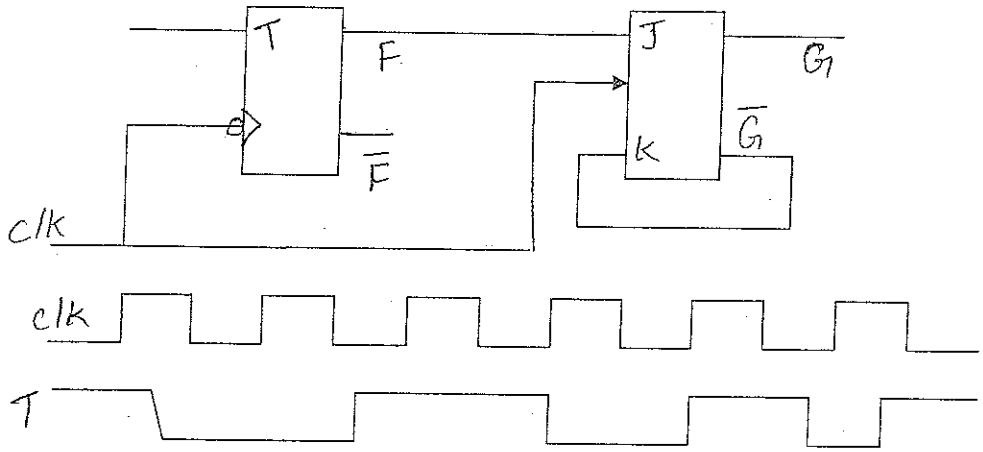
Digital Electronics & Computer Organisation

CS C 391 / INSTR C391 / Test -2 (**Open Book)**

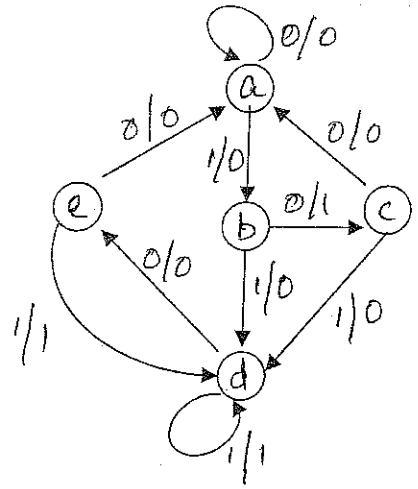
28 – 11 – 10 **Time : 50min.** Max. Marks : 25 **Weightage : 12.5 %**

(Answer all questions)

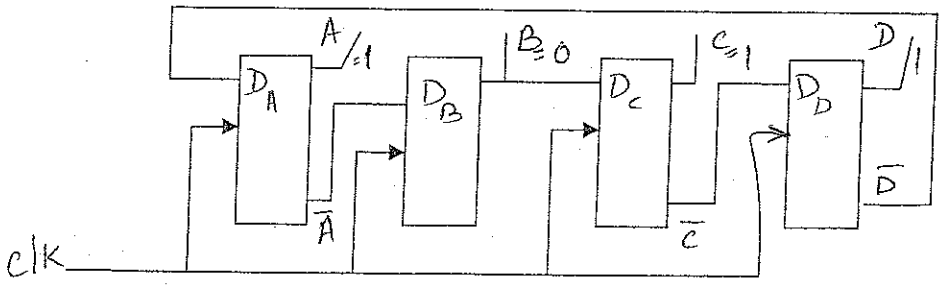
1. In the sequential circuit shown below, plot the output waveforms F and G with respect to the clock for the inputs shown assuming initially F and G were at logic zero (3M+3M)



2. Design a sequential circuit using T flip-flop which will implement the state diagram shown below assuming binary state assignment. (7M)



3 A four bit shift register shown below is initially loaded with a data 1011. Draw the four bit output waveform for six clock pulses. (6M)



4. Derive a PLA programming table for the combinational circuit that squares a 3-bit number. Minimize the number of product terms (6M)

****Good Luck ****

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CS C 391 / INSTR C391

Test -1 **(Closed Book)**

17 – 10 – 10 **Time : 50min.** Max. Marks : 25 **Weightage : 12.5 %**

(Answer all questions. **Calculators are not allowed. Assume positive logic**)

1.a) Implement a NOT, a two-input AND and a two-input OR logic gate using only two-input NAND gates and hence show that the NAND gate is an Universal logic gate. (1+1+2)

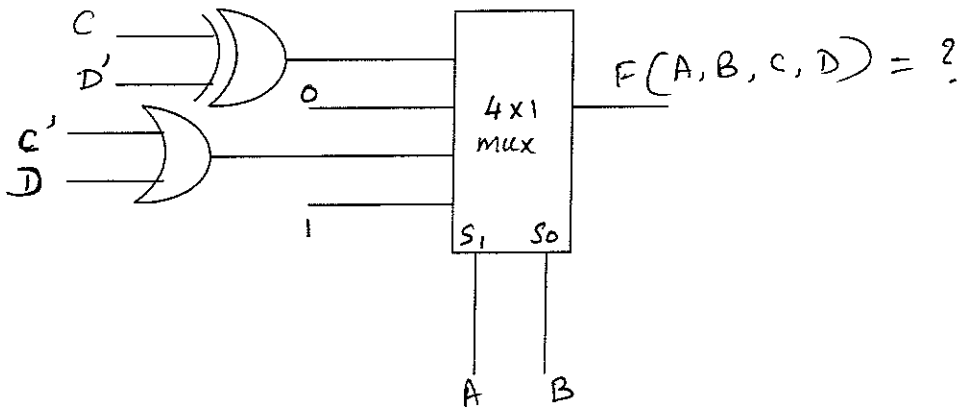
b) Perform the 2's compliment addition using the numbers -12 and +8. Verify the result. (2+1)

2. Design a combinational logic circuit that will cause a warning light to go ***ON*** each time when three or four inputs are low out of 4 binary inputs. It is known that the numbers 0, 5 , 10 and 15 will never occur as inputs. Draw the truth table of this logic circuit. Find out the reduced sum of product expression using K-Map. (2+3)

3a) What is a full adder? Draw the truth table of a full adder. Using full adders alone draw the circuit of a four bit binary parallel adder circuit.

b) Using a 4 bit binary parallel adder (IC 7483) design a BCD to excess-3 code converter (4+2)

4. What is the function implemented in the following circuit? Implement the same logic function using NOR gates alone. (3+4)



****Good Luck ****

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Year III – Semester I 2010 – 2011

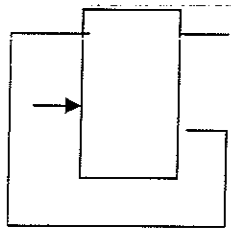
Quiz II(closed Book)

Course No.: **CS / INSTR C 391** Course Title: **DECO**

Date: December 06, 2010 Time: 20 Minutes Max. Marks = 10

(All questions carry two marks each)

1. In a D flip flop the D input is connected as shown below. Draw the out put Q of the flip flop



2. Draw the present state-next state table for the J-K flip-flop. Hence, show that the characteristic equation of the J-K flip-flop is $Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$.

3. In a 4 bit shift register ABCD initially loaded with 1001, What would be the data after three clock pulses if the serial input at A given is 0-1-0-1.

4. Draw the circuit diagram of a JK flip-flop using NAND gates

5. Draw the PLA logic fuse map to implement the two functions given below.
   $F_1(A,B,C) = AB' + BC + A'C$; $F_2(A,B,C) = AC' + BC$

BITS, PILANI – DUBAI SET A

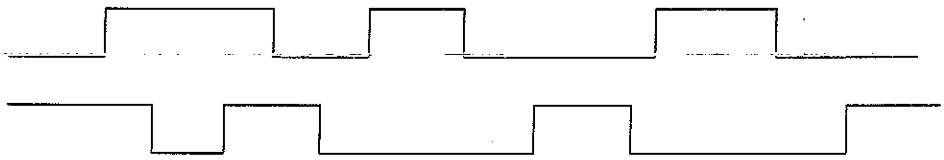
Dubai International Academic city, Dubai
Year III – Semester I 2010 – 2011
QuizI (Closed Book)

Course No.: **CS / EIE C 391** Course Title: **DECO**

Date: November 10, 2010 Time: 25 Minutes Max. Marks = 20

(Answer all Questions. All questions carry two marks each.)

1. In a circuit the inputs A & B are applied to an Ex-OR gate and an AND gate. For the input signals shown below, draw the expected output waveforms from the two logic gates.



2. If you are given 512 x 8 memory ICs and a 3 x 8 decoder, what is the maximum size of memory bank in kilobytes you can address?

3. What is a magnitude comparator? Draw a logic circuit which will compare two single bits A and B

4. Do the following conversion $(123.45)_{10}$ = (----------)$_2$ = (----------)$_8$

5. Using the two's compliment arithmetic perform the following operation on the given decimal number and prove your answer 72 – 91

6. Determine the base of the number for the following operation to be correct

   $(24)_x + (17)_x = (40)_x$

7. Find the Prime Implicants and Essential Prime Implicants of the Boolean function $Y(A,B,C,D) = \Pi\ (2,3,4,5,10,11,12,13)$

8. Implement a half adder using an active low 2 x 4 decoder and minimum no. of logic gates.

9. Draw a ROM programming table to implement the function $F(x) = 2x + 4$ where x is a 3-bit binary number and F(x) is given out in binary. What would be the size of the ROM?

10. Match the following.

i)	Demultiplexer	a) Programmable AND and OR arrays
ii)	PLA	b) 2^n outputs n inputs
iii)	PAL	c) n inputs 2^n outputs
iv)	Encoder	d) 2^n outputs n select lines one input
		e) one output n select lines 2^n input
		f) Programmable AND arrays and fixed OR array

BITS, PILANI – DUBAI SET B

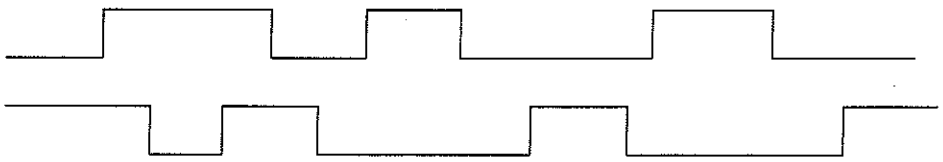
Dubai International Academic city, Dubai
Year III – Semester I 2010 – 2011
QuizI (Closed Book)

Course No.: **CS / EIE C 391** Course Title: **DECO**

Date: November 10, 2010 Time: 25 Minutes Max. Marks = 20

(Answer all Questions. All questions carry two marks each.)

1. In a circuit the inputs A & B are applied to an Ex-NOR gate and an NAND gate. For the input signals shown below, draw the expected output waveform from the two logic gates.



2. If you are given 512 x 4 memory ICs and a 3 x 8 decoder, what is the maximum size of memory bank in kilobytes you can address?

3. Write the Boolean expression to compare two 2-bit words A_1A_0 and B_1B_0

4. Do the following conversion $(543.21)_{10}$ = (----------)$_2$ = (----------)$_8$

5. Using the two's compliment arithmetic perform the following operation on the given decimal number and prove your answer 71 – 90

6. Determine the base of the number for the following operation to be correct

$(23)_x + (14)_x = (40)_x$

7. Find the Prime Implicants and Essential Prime Implicants of the Boolean function $Y(A,B,C,D) = \Pi\ (2,3,4,5,10,11,12,13)$

8. Implement a half adder using an active high 2 x 4 decoder and minimum no. of logic gates.

9. Draw a ROM programming table to implement the function $F(x) = 2x + 3$ where x is a 3-bit binary number and F(x) is given out in binary. What would be the size of the ROM?

10. Match the following.

i)	Demultiplexer	a) Programmable AND and OR arrays
ii)	PLA	b) 2^n outputs n select lines one input
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iv)	Encoder	e) one output n select lines 2^n input
		f) Programmable AND and Fixed OR arrays