BITS, PILANI – DUBAI
FIRST SEMESTER 2010 – 2011
THIRD YEAR - EEE

Course Code: EEE C364 Date:27.12.2010
Course Title: Analog Electronics Max Marks: 70 Marks
Duration: 3 Hours Weightage: 35%
Component: Comprehensive Exam (Closed Book)

Note: 1. This question paper contains 7 Questions and has 4 pages.
2. Assume suitable data if required
3. Answer all Questions

Q1 (a) The input to the zener diode regulator shown in Fig.1 varies from 20V to 40V.Use the ideal characteristics of zener diode and find the maximum and minimum value of Zener current. Assume V_Z = 10V and R=820Ω.

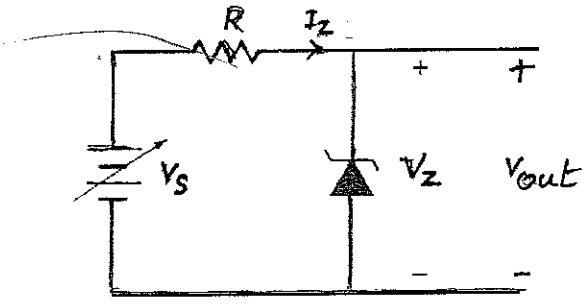


Fig.1

(b) Consider the Common Emitter amplifier circuit with Potential divider biasing arrangement shown in Fig.2. Given Vcc = 9 V, β = 120, R_s = 1kΩ, R_1 =22kΩ , R_2 = 11 kΩ, Rc = 1.2 kΩ, R_L = 4 kΩ and R_E = 1 kΩ , r_0 = ∞ and V_{BE} = 0.7V. Assume all capacitors as short at the given signal frequency. Determine the dc operating point. Draw the ac equivalent circuit for the circuit shown in Fig.2 and find the voltage gain and input resistance. Assume V_T = 25mV in your design.

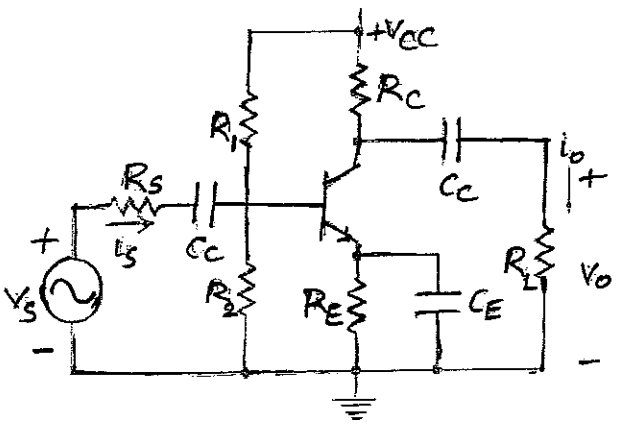


Fig.2 [2M+8 M]

Q2(a) For the circuit shown below(Fig.3),it is required that the current should not exceed 1mA and the output voltage should be such that

$$V_{out} = -(4v_{in1} + 3v_{in2}) \leq |12| \text{ V}.$$

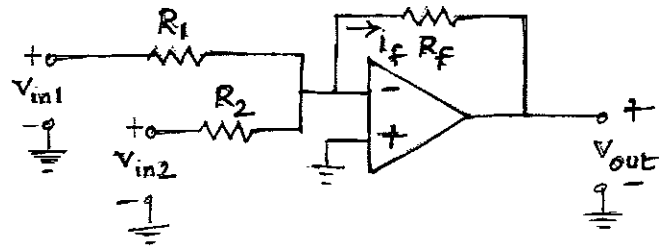


Fig.3

Select appropriate values for resistors R_f, R_1 and R_2 to meet these specifications.

(b) A negative feedback amplifier is shown in Fig.4 . If the gain of the amplifier without feedback is 4000, find the following.

(i) Feedback fraction or feedback ratio

(ii) Overall voltage gain with feedback

(iii) Output voltage If input voltage is 2mV.

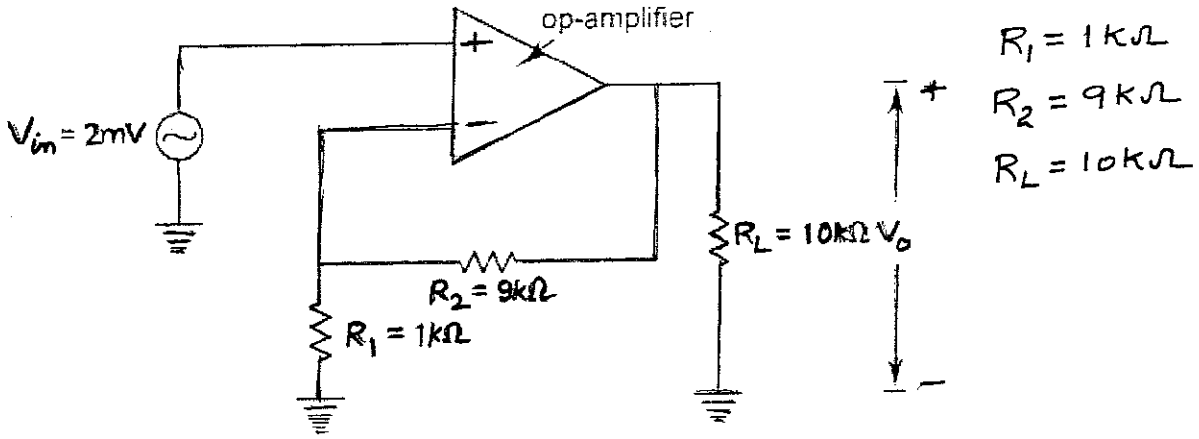


Fig.4 [4M+6M]

Q3 (a) Define the following terms related to phase locked loop circuits

(i) Lock Range and

(ii) Capture Range

(b) Derive the transfer function for the networks given below(Fig.5(a) &Fig.5(b)) and determine the type and order of filter for both circuits.

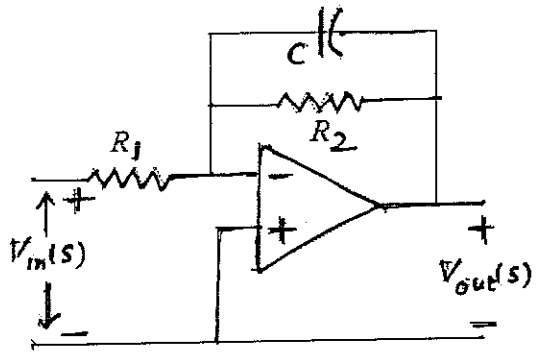


Fig.5(a)

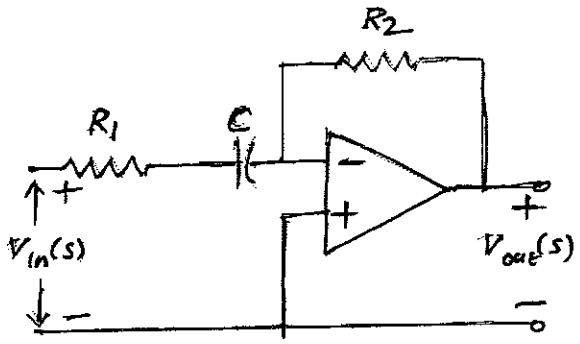


Fig.5(b) [4M + 6M]

Q4 (a) The equivalent circuit of single-tuned amplifier is shown in Fig.6 and has a transconductance $g_m = 30m\Omega^{-1}$ and $R_1 = 500\Omega$.

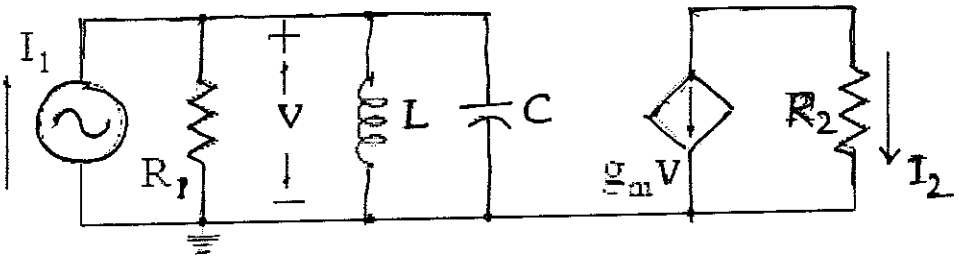


Fig.6

(i) Find the values of L and C so that the half-power bandwidth BW = 10 KHZ and the passband will be centered at 1 MHZ.

(ii) Find the current gain at the resonant frequency and the quality factor Q_0 at parallel resonance.

(b) Draw the functional block diagram of high voltage regulator using IC723 and explain in brief its principle of operation. [4M+6M]

Q5 (a) For the astable multivibrator of Fig.7 the capacitor has the value of 1000 pF.Determine appropriate values for the resistors R_A and R_B so that the circuit will produce a pulse repetition frequency of 100 KHZ with a duty cycle of 75%.

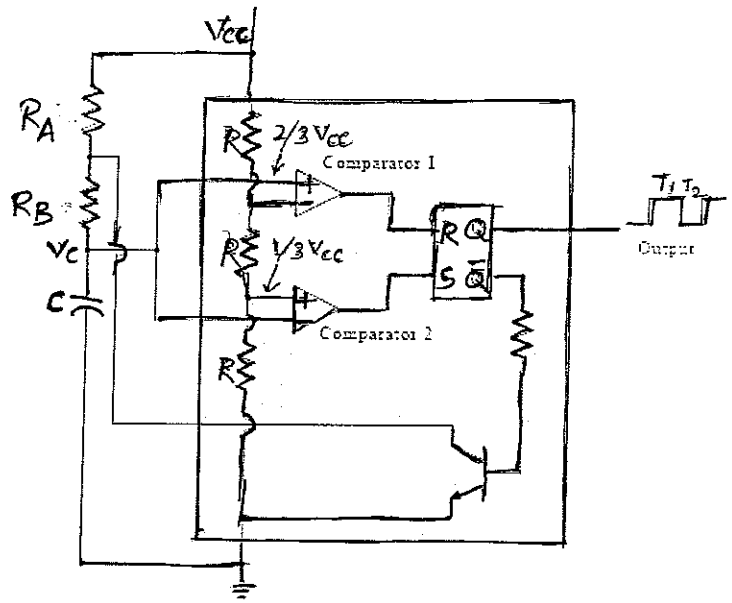


Fig.7

(b) Using a waveform V_i = sinwt ,it is desired to produce a waveform V_o = sin3wt. Draw a schematic of a frequency tripler employing analog multipliers and an opamp subtractor circuit for the above specifications. [6M+4M]

Q6 (a) Distinguish between class A, Class B and Class AB amplifiers.

(b) Show that the maximum power conversion efficiency of Class A power amplifier is limited to 25%. [5M+5M]

Q7(a) Design a D/A converter using resistive divider network for the following specifications:

Input is 3 bit digital inputs and Output is **0** to 5V analog output.

(b) What are all the factors considered for selecting a sensor for a particular application? List the commonly used IC temperature sensors. [5M+5M]

**********End of paper**********

BITS, PILANI – DUBAI
FIRST SEMESTER 2010 – 2011
THIRD YEAR EEE

Course Code: EEE C364 | Date: 28.11.2010
Course Title: Analog Electronics | Max Marks: 30
Duration: 50 Minutes | Weightage: 15%
Component: TEST 2 (Open Book)

Note: **This question paper contains five(5) questions and comprises of 2 pages.**
Answer all Questions. Assume suitable data if required.
Semi log graph sheet is provided along with question paper
Two text books(TB1 and TB2) and handwritten class notes are allowed.

1 Derive the transfer function $V_{out}(s) / V_{in}(s)$ for the network of Fig.1.

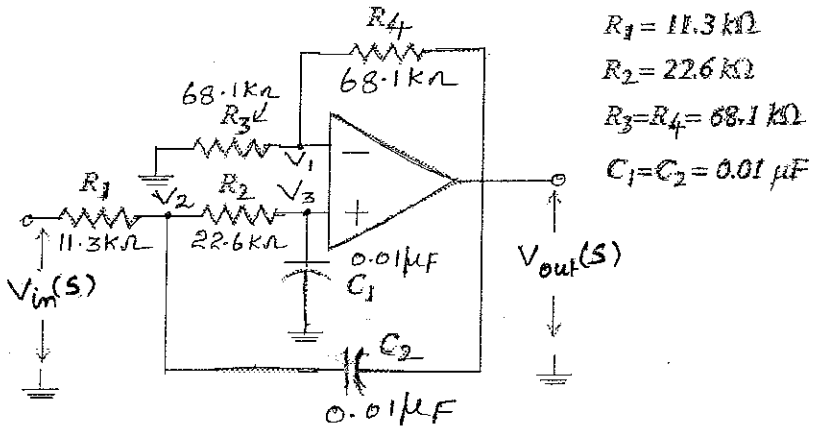
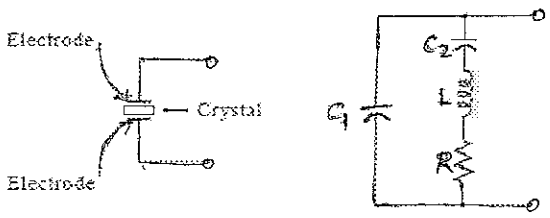


Fig.1 [10 Marks]

2. The figure below shows a Crystal oscillator ( ) and its Equivalent circuit( ).



Prove that

$$\omega_{op} = \sqrt{\frac{C_1 + C_2}{LC_1C_2}}$$

[3 Marks]

P.T.O

3 Design a first order low pass Butterworth filter at a cut off frequency of 2KHZ with a pass band gain of 2. Draw the necessary circuit diagram and plot the frequency response of the low pass filter by expressing gain in decibels. Assume C = 0.01μf,

$R_1 = R_F$ = 10KΩ in your design. Verify the cut off frequency from the graph.

[10 Marks]

4 Explain in brief the function of the circuit shown in Fig.2. Describe the nature of the output V_0. It is desired to obtain a periodic output with a frequency of 1KHZ by choosing 1KΩ for R and 1μf for C. Determine the ratio R1/R2 needed to achieve this. If the circuit of Fig.2 is modified to include an integrator after the output V_0, how would the resulting of output from the integrator look like?

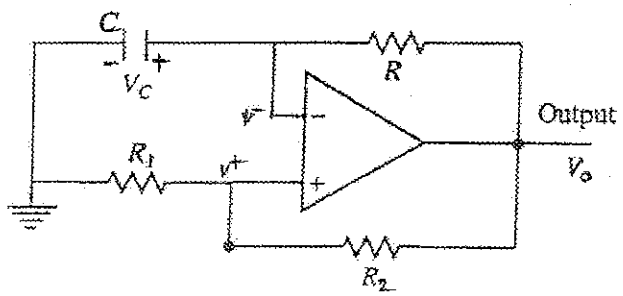
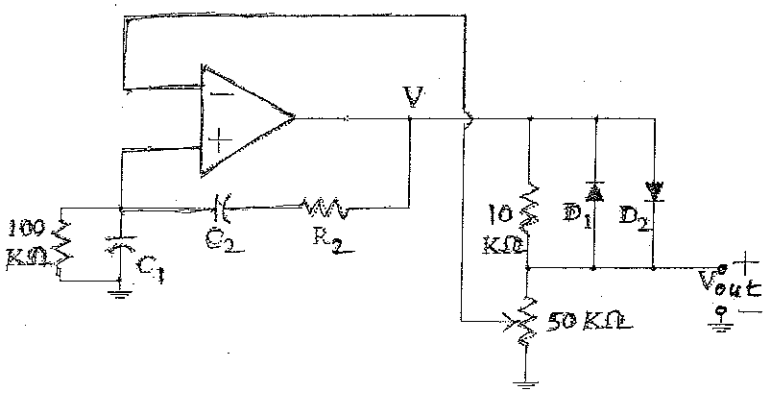


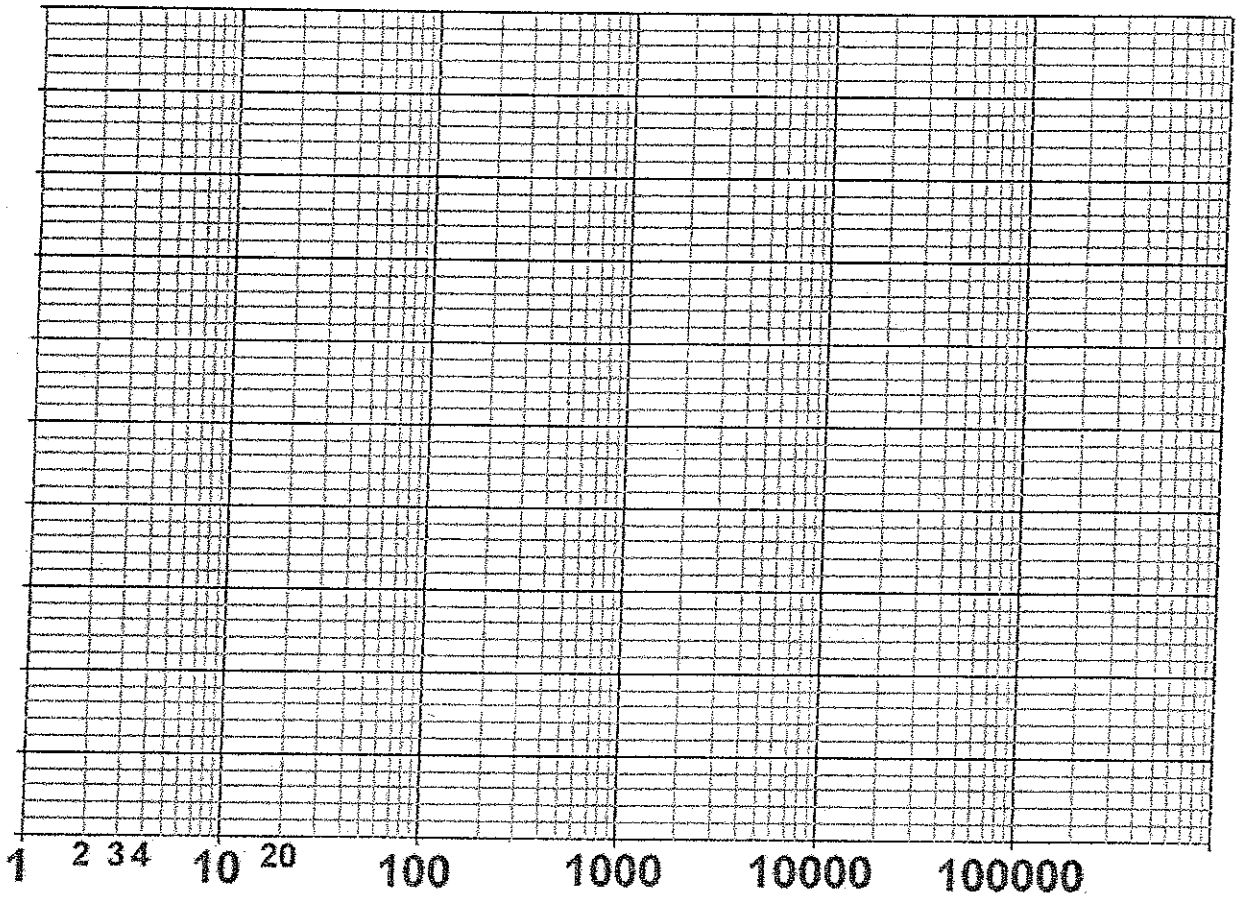
Fig.2 [5 Marks]

5. For the oscillator circuit of Fig.3, what values of R_2, C_1 and C_2 are required to obtain a frequency of approximately 1KHZ?



[2 Marks]

Fig. 3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BITS, PILANI – DUBAI
FIRST SEMESTER 2010 – 2011
THIRD YEAR EEE

Course Code: EEE C364
Course Title: Analog Electronics
Duration: 50 Minutes
Component: TEST 1 (Closed Book)

Date: 17.10.2010
Max Marks: 30
Weightage: 15%

Note: This question paper contains four (4) questions and comprises of 2 pages.
Answer all Questions. Assume suitable data if required.

1 Consider the Common Emitter amplifier circuit with Potential divider biasing arrangement shown in Fig.1. Given Vcc = 15 v, $\beta = 100$, $R_s = 1k\Omega$, $R_1 = 10k\Omega$, $R_2 = 5\ k\Omega$, $Rc = 4\ k\Omega$, $R_L = 4\ k\Omega$ and $R_E = 2\ k\Omega$, $r_0 = \infty$ and $V_{BE} = 0.7V$. Assume all capacitors as short at the given signal frequency. Determine the dc operating point. [5 Marks]

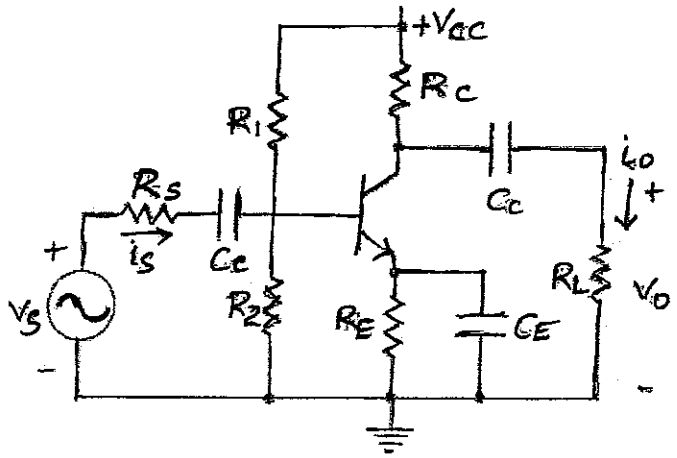

Fig.1

2. What output voltage results for an input of 1.25 v in the circuit of Fig.2

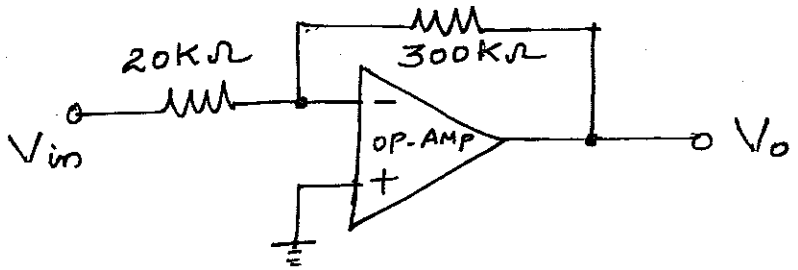

FIG.2 [5 Marks]

3 . For the circuit shown in Fig.3 compute output voltage v_{out2}

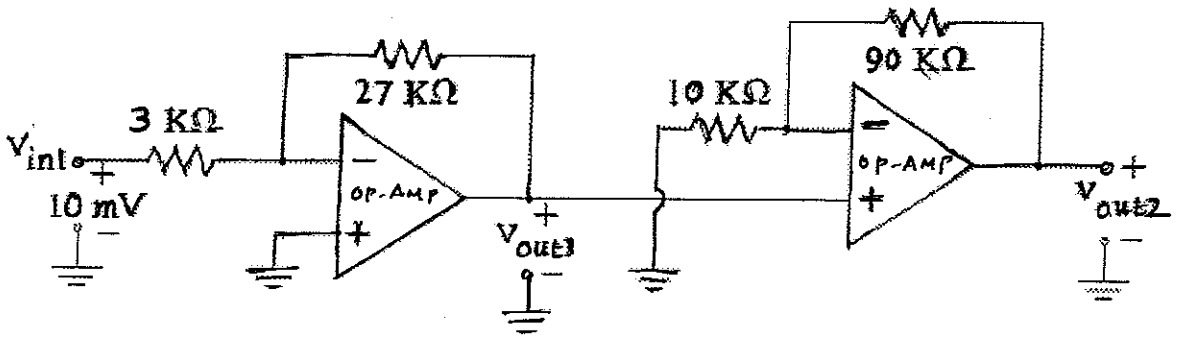

Fig.3 [10 Marks]

4. Assuming the op-amp to be ideal, derive **Vo/Vs** for the circuit shown in Fig.4

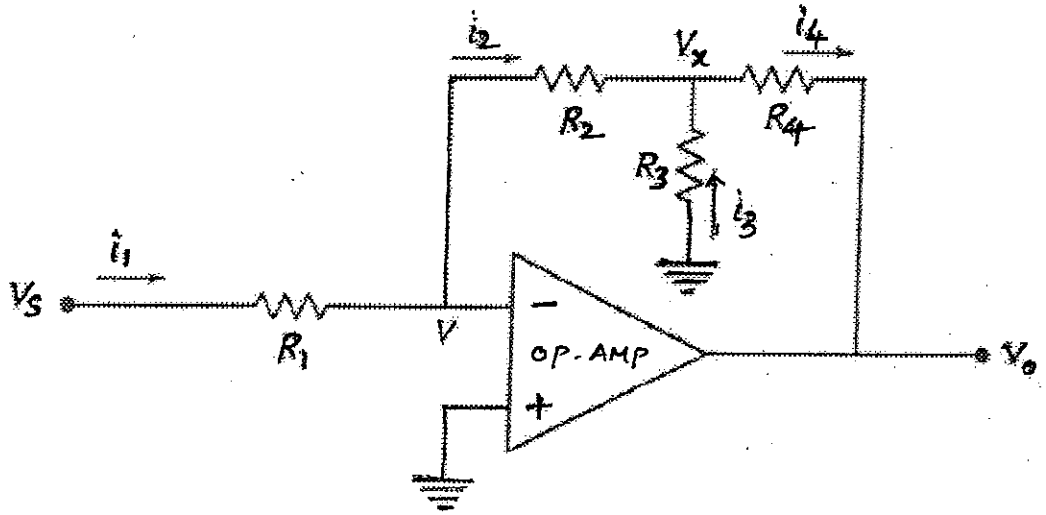

FIG.4 [10 Marks]

**********THE END**********

BITS, PILANI – DUBAI
FIRST SEMESTER 2010 – 2011

Course Code: EEE C364 Date: 6.12.2010
Course Title: Analog Electronics Max Marks: 10
Duration: 20 Minutes Weightage: 5%
Component: QUIZ 2 (Closed Book)
ID NUMBER: NAME OF THE STUDENT:

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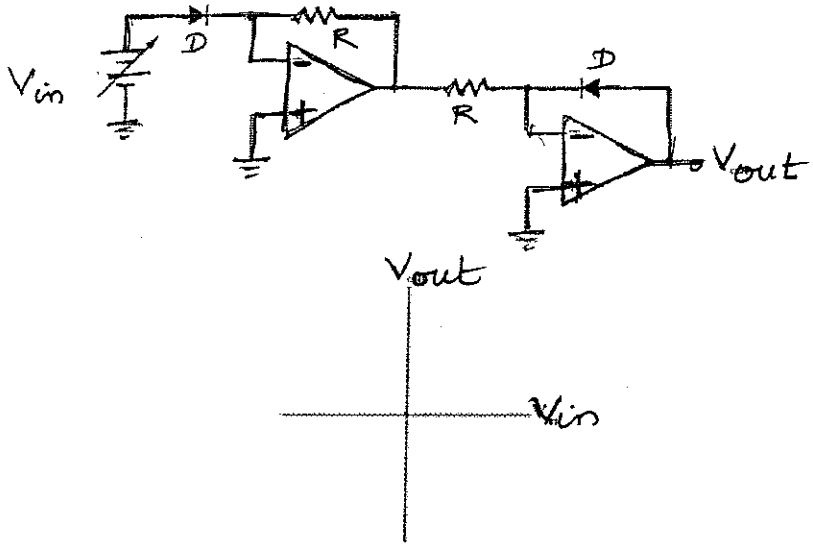
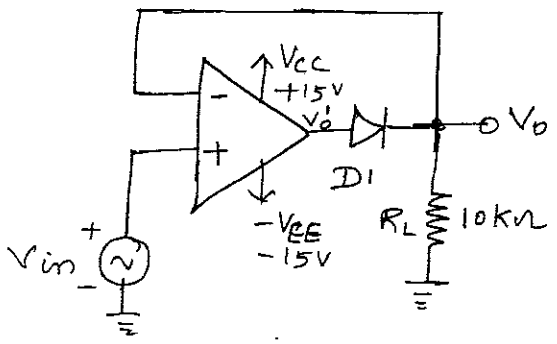
1. Plot the transfer function (V_{out} versus V_{in}) for this following opamp circuit



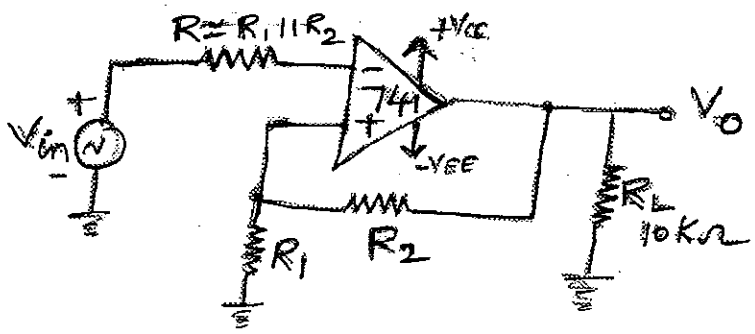
What type of mathematical function is represented by the above circuit? (2M)

2. In the circuit of the figure shown below, V_{in} = 200mV peak-to-peak sine wave at **100HZ. Briefly** describe the operation of the circuit (**write only the key points**) and also draw the input and output waveforms **(2M)**



3. Draw the circuit diagram of positive clipper circuit and sketch the input and output waveforms. (2M)

4. In the circuit of Figure shown below, R_1 = 95Ω, R_2 = 50kΩ, V_{in} = 1 V Peak to peak sine wave and the op amp is 741 with saturation voltages of +Vsat =14V and –Vsat = -14V. Find the threshold voltages Vut and Vlt. Also draw the necessary waveform for both input and output voltages.



(3M)

5. Clamper circuits are sometimes referred to as ----------circuits. Does a "clamper" circuit change the shape of a voltage waveform, like a "clipper" circuit does? Justify. **(Write only the key point in your answer).** (1M)

BITS, PILANI – DUBAI
FIRST SEMESTER 2010 – 2011

Course Code: EEE C364 Date: 10.11.2010
Course Title: Analog Electronics Max Marks: 10
Duration: 20 Minutes Weightage: 5%
Component: QUIZ1 (Closed Book) SET A

ID NUMBER: NAME OF THE STUDENT:

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1. Calculate the gain of a negative feedback amplifier with an internal gain A = 125 and feedback factor β = 1/10. [2Marks]

2. Fig.1 shows the schematic of a typical two op-amp instrumentation amplifier circuit. Show that $V_o = (V_{i2} - V_{i1})\left(1 + \frac{R_4}{R_3}\right)$ for $R_1 = R_4$ & $R_2 = R_3$

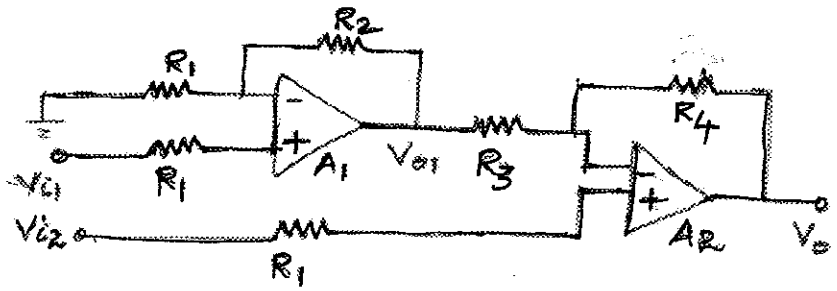

Fig.1

[4 Marks]

P.T.O

3. A shunt-series feedback amplifier represented by Fig.2 and using an ideal basic current amplifier operates with Is = 100μA, I_f = 95 μA and I_o = 10mA. What are the corresponding values of A and β? Include correct units for each.

[4 Marks]

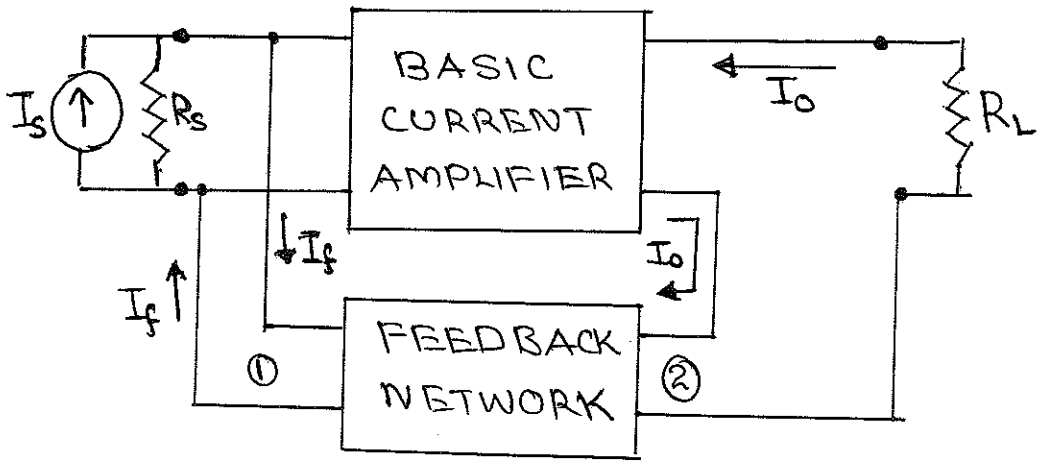

Fig. 2